LINGAYAS INSTITUTE OF MANAGEMENT AND TECHNOLOGY

Department of Electronics and Communication Engineering

Course Handout for II Year B. Tech PROGRAM

A.Y.2021 – 22, I[st] Semester

Course Name	:	**ELECTRONIC DEVICES & CIRCUITS**
Course Code	:	PC01
L-T-P structure	:	3 – 1 – 2
Course Credits	:	03
Course Instructor	:	Dr. D.S.P. PHANI KISHORE

Course Objective:

The main objectives of this course are:

- To learn and understand the basic concepts of semiconductor physics.
- Study the physical phenomena such as conduction, transport mechanism and electrical characteristics of different diodes.
- To learn and understand the application of diodes as rectifiers with their operation and characteristics with and without filters are discussed.
- Acquire knowledge about the principle of working and operation of Bipolar Junction Transistor and Field Effect Transistor and their characteristics.
- To learn and understand the purpose of transistor biasing and its significance.
- Small signal equivalent circuit analysis of BJT and FET transistor amplifiers and compare different configurations. on types of Sensors/ Transducers working principles, selection procedures, applications of sensing systems.

Course Rationale:

The course is taking by Second year students of ECE students to acquire the knowledge about the fundamental principles of electronic devices and circuits from the earlier silicon substrate version to latest insulated gate technology which will enabling the student to implement in their real-world applications. By learning the different electronic devices and their characteristics through theoretical and practical sessions, learners are well suitable to design the circuits and systems for the societal related problems. In this course the learners are aimed five outcomes which provide the knowledge about the fundamental principles of different electronic devices, circuits and their working and designing principles, selection criteria and applications.

Course Outcomes (CO):

CO No:	CO	PO	BTL
1	To Understand the formation of p-n junction and how it can be used as a PN junction as diode in different modes of operation and special functions PN junctions	PO1, PO2	UNDERSTAND
2	To Know the construction, working principle of rectifiers with and without filters with relevant expressions and necessary comparisons.	PO1, PO2	ANALYSE
3	To Understand the construction, principle of operation of transistors, BJT and FET with their V-I characteristics in different configurations.	PO1, PO2, PSO1	UNDERSTAND
4	To Know the need of transistor biasing, various biasing techniques for BJT and FET and stabilization concepts with necessary expressions	PO1, PO2, PSO1	ANALYSE
5	To Perform the analysis of small signal low frequency transistor amplifier circuits using BJT	PO1, PO2	APPLY

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COURSE OUTCOME INDICATORS (COI):

CO No.	COI-1	COI-2
1	To Understand the formation of p-n junction, PN Diode, Modes	To understand about Special Semiconductor diodes
2	To Know the construction, working principle of rectifiers with and without filters	Using relevant expressions and necessary comparisons differentiation among the filter circuits
3	To Understand the construction, principle of operation of transistors, BJT and FET	The V-I characteristics and different configurations of BJT and FET
4	To Know the need of transistor biasing, biasing techniques for BJT and FET	Stabilization concepts with necessary expressions.
5	To Perform the analysis of small signal low frequency transistor amplifier circuits using BJT	To Perform the analysis of small signal low frequency transistor amplifier circuits using FET

PROGRAM OUTCOMES (POs)

a. **Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.**

b. **Problem Analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.**

PROGRAM SPECIFIC OUTCOMES (PSO)

At the end of the program, the student

PSO 1: should be able to understand the concepts of Electronics & Communication engineering and their applications in the field of semiconductor technology, consumer electronics, embedded system, communication/ networking and other relevant areas.

CO-PO Mapping Matrix

COs	PO1	PO2	PSO1
CO1	3	2	
CO2	3	2	
CO3	3	2	2
CO4	3	2	2
CO5	3	2	

3: Substantially 2: Moderately 1: Poor

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SYLLABUS:

UNIT – I

Review of Semiconductor Physics:

Hall effect, continuity equation, law of junction, Fermi Dirac function, Fermi level in intrinsic and extrinsic Semiconductors

Junction Diode Characteristics: energy band diagram of PN junction Diode, Open circuited p-n junction, Biased p-n junction, p-n junction diode, current components in PN junction Diode, diode equation, V-I Characteristics, temperature dependence on VI characteristics, Diode resistance, Diode capacitance.

UNIT-II:

Special Semiconductor Devices: Zener Diode, Breakdown mechanisms, Zener diode applications,

LED, Varactor Diode, Photodiode, Tunnel Diode, UJT, PN-Diode, SCR. Construction, operation, and V-I characteristics.

Rectifiers and Filters: Basic Rectifier setup, half wave rectifier, full wave rectifier, Bridge rectifier, derivations of characteristics of rectifiers, rectifier circuits-operation, input and output waveforms, Filters, Inductor filter (Series inductor), Capacitor filter(Stunt inductor), π- Filter, comparison of various filter circuits in terms of ripple factors.

UNIT-III: Transistor Characteristics:

BJT: Junction transistor, transistor current components, transistor equation, transistor configurations, transistor as an amplifier, characteristics of transistor in Common Base, Common Emitter and Common Collector configurations, Ebers-Moll model of a transistor, punch through/reach through, Photo transistor, typical transistor junction voltage values.

FET: FET types, construction, operation, characteristics μ, gm, rd parameters, MOSFET-types, construction, operation, characteristics, comparison between JFET and MOSFET.

UNIT- IV: Transistor Biasing and Thermal Stabilization: Need for biasing, operating point, load line analysis, BJT biasing- methods, basic stability, fixed bias, collector to base bias, self-bias, Stabilization against variations in VBE, Ic, and β, Stability factors, (S,S',S''), Bias compensation, Thermal runaway, Thermal stability. FET Biasing-methods and stabilization.

UNIT-V: Small Signal Low Frequency Transistor Amplifier Models:

BJT: Two port network, Transistor hybrid model, determination of h-parameters, conversion Of h-parameters, generalized analysis of transistor amplifier model using h-parameters, Analysis of CB, CE and CC amplifiers using exact and approximate analysis, Comparison of Transistor amplifiers.

FET: Generalized analysis of small signal model, Analysis of CG, CS and CD amplifiers, comparison of FET amplifiers.

Textbooks:

1. Electronic Devices and Circuits-J. Millman, C. Halkias, Tata Mc-Graw Hill, Second Edition, 2007
2. Electronic Devices and Circuits-K. Lal Kishore, BS Publications, Fourth Edition, 2016.
3. Electronics devices & circuit theory-Robert L. Boylestad and Loui Nashelsky, Pearson / Prentice Hall, tenth edition, 2009

References:

1. Integrated Electronics-J. Millman, C. Halkias, Tata Mc-Graw Hill, Second Edition,2009
2. Electronic Devices and Integrated Circuits – B.P. Singh, Rekha, Pearson publications
3. Electronic Devices and Circuits-Salivahanan, Kumar, Vallava raj, Tata Mc-Graw Hill, 4thEdition,2008.

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COURSE DELIVERY PLAN:

S. No	CO	COI	Topic (s)	Teaching-Learning Methods	Evaluation Components
1	--	--	Introduction to EDC course, Syllabus discussion COs and their significance demonstration, Assessment	Chalk & Talk	NA
2	1	1	Semiconductors and classification, Energy band theory	Chalk & Talk/ PPT	Quiz, Home Assignments, CBT, OBT, Poll questions, MID-1, SEM End Exam
3	1	1	Hall effect, continuity equation	Chalk & Talk/PPT	
4	1	1	law of junction, Fermi Dirac function, Fermi level in intrinsic and extrinsic Semiconductors	Chalk & Talk/PPT	
5	1	1	Junction Diode Characteristics	Chalk & Talk/PPT	
6	1	1	Energy band diagram of PN junction Diode	Chalk & Talk/PPT	
7	1	1	Open circuited p-n junction, Biased p-n junction	Chalk & Talk/PPT	
8	1	1	p-n junction diode, characteristics	Chalk & Talk/PPT	
9	1	1	current components in PN junction Diode	Chalk & Talk/PPT	
10	1	1	Diode equation, temperature dependence	Chalk & Talk/PPT	
11	1	1	Diode resistance and capacitance	Chalk & Talk/PPT	
12	1	2	Zener Diode, Breakdown mechanisms, Zener diode applications	Chalk & Talk/PPT	
13	1	2	LED, Varactor Diode, Photodiode, Tunnel Diode	Chalk & Talk/PPT	
14	1	2	UJT, PN-Diode, SCR, and its V-I characteristics	Chalk & Talk/PPT	
15	2	1	Basic Rectifier setup, half wave rectifier	Chalk & Talk/PPT	
16	2	1	Full wave rectifier, Bridge rectifier	Chalk & Talk/PPT	
17	2	1	derivations of characteristics of rectifiers, rectifier circuits-operation, input, and output waveforms	Chalk & Talk/PPT	
18	2	1	derivations of characteristics of rectifiers, rectifier circuits-operation, input, and output waveforms	Chalk & Talk/PPT	
19	2	2	Filters, Inductor filter (Series inductor)	Chalk & Talk/PPT	
20	2	2	Capacitor filter (Stunt Inductor), π- Filter, comparison of various filter circuits in terms of ripple factors.	Chalk & Talk/PPT	
21	3	1	BJT: Junction transistor, transistor current components,	Chalk & Talk/PPT	
22	3	1	transistor equation, transistor configurations	Chalk & Talk/PPT	
23	3	1	transistor as an amplifier	Chalk & Talk/PPT	Quiz, Home Assignments, CBT, OBT, Poll questions, MID-2, Sem End
24	3	1	FET: and its current components,	Chalk & Talk/PPT	
25	3	1	Current equation, configurations	Chalk & Talk/PPT	
26	3	1	FET as an amplifier	Chalk & Talk/PPT	
27	3	2	characteristics of transistor in Common Base, Common Emitter and Common Collector configurations	Chalk & Talk/PPT	
28	3	2	characteristics of transistor in Common Base, Common Emitter and Common Collector configurations	Chalk & Talk/PPT	
29	3	2	Ebers-Moll model of a transistor, punch through/reach through	Chalk & Talk/PPT	
30	3	2	Photo transistor, typical transistor junction voltage values	Chalk & Talk/PPT	
31	3	2	characteristics μ, gm, rd parameters,	Chalk & Talk/PPT	
32	3	2	MOSFET-types, construction, operation	Chalk & Talk/PPT	
33	3	2	characteristics, comparison between JFET and MOSFET	Chalk & Talk/PPT	
34	4	1	Need for biasing, operating point	Chalk & Talk/PPT	
35	4	1	load line analysis	Chalk & Talk/PPT	
36	4	1	BJT biasing- methods	Chalk & Talk/PPT	
37	4	1	BJT biasing- methods	Chalk & Talk/PPT	

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38	4	2	basic stability	Chalk & Talk/PPT	Exam
39	4	2	Stabilization against variations in VBE, Ic, and β, Stability factors	Chalk & Talk/PPT	
40	4	2			
41	4	2	(S, S', S''), Bias compensation, Thermal runaway, Thermal stability	Chalk & Talk/PPT	
42	4	2	FET Biasing-methods and stabilization.	Chalk & Talk/PPT	
43	4	2	FET methods of stabilization.	Chalk & Talk/PPT	
44	5	1	BJT: Two port network, Transistor hybrid model	Chalk & Talk/PPT	
45	5	1	determination of h-parameters	Chalk & Talk/PPT	
46	5	1	Conversion Of h-parameters	Chalk & Talk/PPT	
47	5	1	generalized analysis of transistor amplifier model using h-parameters	Chalk & Talk/PPT	
48	5	1	Analysis of CB, CE and CC amplifiers using exact and approximate analysis	Chalk & Talk/PPT	
49	5	1			
50	5	2	FET: Generalized analysis of small signal model	Chalk & Talk/PPT	
51	5	2	Analysis of CG, CS and CD amplifiers	Chalk & Talk/PPT	
52	5	2			
53	5	2	Comparison of FET amplifiers	Chalk & Talk/PPT	

LECTURE PLAN : ELECTRONIC DEVICES & CIRCUITS II-I AY: 2021 – 2022

S. No	Date planned	Topic (s)	Date completed	Teaching-Learning Methods	Remarks
1	05.09.2021	Introduction to EDC course, Syllabus discussion COs and their significance demonstration, Assessment		Chalk & Talk	
2	06.09.2021 07.09.2021	Semiconductors and classification, Energy band theory		Chalk & Talk/ PPT	
3	08.09.2021	Hall effect, continuity equation		Chalk & Talk/PPT	
4	09.09.2021 12.09.2021	law of Junction, Fermi Dirac function, Fermi level in intrinsic and extrinsic Semiconductors		Chalk & Talk/PPT	
5	13.09.2021	Junction Diode Characteristics		Chalk & Talk/PPT	
6	14.09.2021	Energy band diagram of PN junction Diode		Chalk & Talk/PPT	
7	16.09.2021	Open circuited p-n junction, Biased p-n junction		Chalk & Talk/PPT	
8	19.09.2021	p-n junction diode, characteristics		Chalk & Talk/PPT	
9	20.09.2021 21.09.2021	current components in PN junction Diode		Chalk & Talk/PPT	
10	22.09.2021	Diode equation, temperature dependence		Chalk & Talk/PPT	
11	23.09.2021	Diode resistance and capacitance		Chalk & Talk/PPT	
12	26.09.2021	Zener Diode, characteristics		Chalk & Talk/PPT	
13	27.09.2021	Breakdown mechanisms		Chalk & Talk/PPT	
14	28.09.2021	Zener diode applications: voltage regulator		Chalk & Talk/PPT	
15	29.09.2021	LED, Varactor Diode		Chalk & Talk/PPT	
16	30.09.2021	Photodiode, Tunnel Diode		Chalk & Talk/PPT	
17	07.10.2021	UJT, PN-Diode		Chalk & Talk/PPT	
18	10.10.2021	SCR, and its V-I characteristics		Chalk & Talk/PPT	
19	11.10.2021	Basic Rectifier setup, Half wave rectifier			
20	12.10.2021	derivations of characteristics of half-wave rectifiers, rectifier circuits-operation, input, and output waveforms			
21	13.10.2021	Full wave rectifier, Bridge rectifier		Chalk & Talk/PPT	
21	14.10.2021	derivations of characteristics of rectifiers, rectifier circuits-operation, input, and output waveforms		Chalk & Talk/PPT	
23	17.10.2021	Filters, Inductor filter (Series inductor)		Chalk & Talk/PPT	
24	18.10.2021	Capacitor filter (Stunt inductor), π- Filter, comparison of various filter circuits in terms of ripple factors.		Chalk & Talk/PPT	
25	19.10.2021	BJT: Junction transistor, transistor current components,		Chalk & Talk/PPT	
26	20.10.2021	transistor equation, transistor configurations		Chalk & Talk/PPT	
27	21.10.2021	transistor as an amplifier		Chalk & Talk/PPT	
		MID – I			
28	31.10.2021	FET: and its current components,		Chalk & Talk/PPT	
29	01.11.2021	Current equation, configurations		Chalk & Talk/PPT	
30	02.11.2021	FET as an amplifier		Chalk & Talk/PPT	
31	03.11.2021 04.11.2021	characteristics of transistor in Common Base, Common Emitter and Common Collector configurations		Chalk & Talk/PPT	
32	07.11.2021	characteristics of transistor in Common Base, Common		Chalk & Talk/PPT	

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	08.11.2021	Emitter and Common Collector configurations			
33	09.11.2021 10.11.2021	Ebers-Moll model of a transistor, punch through/reach through		Chalk & Talk/PPT	
34	11.11.2021	Photo transistor, typical transistor junction voltage values		Chalk & Talk/PPT	
35	14.11.2021	characteristics μ, gm, rd parameters,		Chalk & Talk/PPT	
36	15.11.2021	MOSFET-types, construction, operation		Chalk & Talk/PPT	
37	16.11.2021	characteristics, comparison between JFET and MOSFET.		Chalk & Talk/PPT	
38	17.11.2021	Need for biasing, operating point		Chalk & Talk/PPT	
39	18.11.2021	load line analysis		Chalk & Talk/PPT	
40	21.11.2021	BJT biasing- methods		Chalk & Talk/PPT	
41	22.11.2021	BJT biasing- methods		Chalk & Talk/PPT	
42	23.11.2021	basic stability		Chalk & Talk/PPT	
43	24.11.2021	Stabilization against variations in VBE, Ic, and β, Stability factors		Chalk & Talk/PPT	
44	25.11.2021				
45	28.11.2021	(S, S', S''), Bias compensation, Thermal runaway, Thermal stability		Chalk & Talk/PPT	
46	29.11.2021	FET Biasing-methods and stabilization.		Chalk & Talk/PPT	
47	30.11.2021	FET methods of stabilization.		Chalk & Talk/PPT	
48	01.12.2021	BJT: Two port network, Transistor hybrid model		Chalk & Talk/PPT	
49	02.12.2021	determination of h-parameters		Chalk & Talk/PPT	
50	05.12.2021	Conversion Of h-parameters		Chalk & Talk/PPT	
51	06.12.2021	generalized analysis of transistor amplifier model using h-parameters		Chalk & Talk/PPT	
52	07.12.2021	Analysis of CB, CE and CC amplifiers using exact and approximate analysis		Chalk & Talk/PPT	
53	08.12.2021				
54	09.12.2021	FET: Generalized analysis of small signal model		Chalk & Talk/PPT	
55	12.12.2021	Analysis of CG, CS and CD amplifiers		Chalk & Talk/PPT	
56	13.12.2021				
57	14.12.2021	Comparison of FET amplifiers		Chalk & Talk/PPT	
58	15.12.2021	Revision of CO 1, 2		Chalk & Talk/PPT	
59	16.12.2021	Revision of CO 3, 4, 5		Chalk & Talk/PPT	
60	19.12.2021	Model Papers		Chalk & Talk/PPT	
MID – II					

EVALUATION PLAN:

S. No	Component	Assessment type			Date	CO				Evaluation done by
						1	2	3	4	
1	Theory	Internal Assessment	MID-1	Descriptive	24.10.2021 to 29.10.2021	X	X			Dr DSPPK
			MID-2		19.11.2021 to 24.11.2021			X	X	
			Quiz-1	Objective type	24.10.2021 to 29.10.2021	X	X			ONLINE
			Quiz-2		19.11.2021 to 24.11.2021			X	X	
			A-1	Home Assignments for each CO		X				Dr DSPPK
			A-2				X			
			A-3					X		
			A-4						X	
		External Assessment	Univ. Exam	Descriptive type	02.01.2023 to 14.01.2023	X	X	X	X	University

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Self Learning:

https://www.youtube.com/watch?v=f5lpIHrBvtQ
https://www.youtube.com/watch?v=USrY0IspDLg
https://www.youtube.com/watch?v=cAu_QvGrsMI
https://www.youtube.com/watch?v=JdLJDnnfHXw
https://www.youtube.com/watch?v=MZPeRlst8rQ
https://www.youtube.com/watch?v=37-XWSe26LM
https://www.youtube.com/watch?v=J4gO7PJ_nzQ
https://www.youtube.com/watch?v=dIx9VKV0hjo
https://www.youtube.com/watch?v=PMOa59G7Yus

Course Team members, Chamber Consultation Hours and Chamber Venue details:

S. No.	Name of Faculty	Chamber Consultation Day(s)	Chamber Consultation Timings for each day	Chamber Consultation Room No:	Signature of Course faculty
1	Dr DSP PHANI KISHORE	All Weekdays	After 3pm	215	

Time Table

Day	8.30	9.20	10.20	11.10	12.30	1.10	2.10	3.00
MON		SS			EDC			
TUE					EDC		EDC LAB	
WED	SS	EDC						
THU			EDC					SS
FRI		EDC	SS					
SAT	SS					SS		

Signature of COURSE INSTRUCTOR:

Recommended by HEAD OF DEPARTMENT:

Approved By: Incharge ACADEMICS

(Sign with Office Seal)

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INSTRUCTION DIVISION

III YEAR FIRST SEMESTER 2021– 2022

(BIOMETRIC SYSTEM OF ATTENDENCE IS MANDATORY AS PER NOMS OF GOVT. OF AP AND JNTUK)

Course Handout

In addition to Part I (General Handout for all courses appended to the Time Table) this portion further specific details regarding the course.

L	T	P	C
3	0	0	3

Course Code	:	**R1931042**
Course Title	:	**MICROPROCESSOR AND MICROCONTROLLERS**
Instructor-in-charge	:	**Prof. T. HEMALATHA**

Scope and objective of the course: The objective of this course is:

Course objectives: The main objectives of this course are

- To acquire knowledge on microprocessors and microcontrollers.
- To select processors based on requirements.
- To acquire the knowledge on interfacing various peripherals, configure and develop programs to interface peripherals/sensors.
- To develop programs efficiently on ARM Cortex processors and debug

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SYLLABUS

UNIT–I

Introduction: Basic Microprocessor architecture, Harvard and Von Neumann architectures with examples, Microprocessor Unit versus Microcontroller Unit, CISC and RISC architectures.

8086 Architecture: Main features, pin diagram/description, 8086 microprocessor family, internal architecture, bus interfacing unit, execution unit, interrupts and interrupt response, 8086 system timing, minimum mode and maximum mode configuration.

UNIT–II

8086 Programming: Program development steps, instructions, addressing modes, assembler directives, writing simple programs with an assembler, assembly language program development tools.

UNIT-III

8086 Interfacing: Semiconductor memories interfacing (RAM, ROM), Intel 8255 programmable peripheral interface, Interfacing switches and LEDS, Interfacing seven segment displays, software and hardware interrupt applications, Intel 8251 USART architecture and interfacing, Intel 8237a DMA controller, stepper motor, A/D and D/A converters, Need for 8259 programmable interruptcontrollers.

UNIT-IV

Intel 8051 MICROCONTROLLER

Architecture, Hardware concepts, Input / output ports and circuits, external memory, counters / timers, serial data input/output, interrupts.

Assembly language programming: Instructions, addressing modes, simple programs. Interfacing to 8051: A/D and D/A Convertors, Stepper motor Interface, keyboard, LCD Interfacing, Traffic light control.

UNIT–V

ARM Architectures and Processors: ARM Architecture, ARM Processors Families, ARM Cortex-M Series Family, ARM Cortex-M3 Processor Functional Description, functions and interfaces.

Programmers Model – Modes of operation and execution, Instruction set summary, System address map, write buffer, bit-banding, processor core register summary, exceptions.

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ARM Cortext-M3 programming – Software delay, Programming techniques, Loops, Stack and Stack pointer, subroutines and parameter passing, parallel I/O, Nested Vectored Interrupt Controller – functional description and NVIC programmers' model.

Study Material:

TEXT BOOKS:

1. Microprocessors and Interfacing – Programming and Hardware by Douglas V Hall, SSSP Rao, Tata McGraw Hill Education Private Limited, 3rd Edition, 1994.
2. The 8051 Microcontrollers and Embedded systems Using Assembly and C, Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay; Pearson 2-Edition, 2011.
3. The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by JosephYou.

REFERENCE BOOKS:

1. 1. Embedded Systems Fundamentals with Arm Cortex-M based Microcontrollers: A Practical Approach in English, by Dr. Alexander G. Dean, Published by Arm Education Media,2017.
2. Cortex -M3 Technical Reference Manual.

UNIT/MODULE	TOPIC	Duration	Textbook/Reference book/Source...
UNIT-1			
1.0	Basic Microprocessor architecture	50/60 mins	T1, R1
1.1	Microprocessor Unit versus Microcontroller Unit	50/60 mins	T1, R1
1.2	Harvard and Von Neumann architectures with examples, CISC and RISC architectures	50/60 mins	T1, R1
1.3	8086 Architecture: Main features	50/60 mins	T1, R1
1.4	Pin diagram/description	50/60 mins	T1, R1
1.5	Pin diagram/description	50/60 mins	T1, R1
1.6	8086 microprocessor family	50/60 mins	T1, R1
1.7	8086 Internal Architecture – BIU	50/60 mins	T1, R1
1.8	8086 Internal Architecture – EU	50/60 mins	T1, R1
1.9	Interrupts and interrupt responses	50/60 mins	T1, R1
1.10	8086 system timing	50/60 mins	T1, R1
1.11	Minimum mode configuration	50/60 mins	T1, R1
1.12	Maximum mode configuration	50/60 mins	T1, R1

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UNIT-2			
2.0	8086 Programming: Program development steps	50/60 mins	T2, R1
2.1	Instructions	50/60 mins	T2, R1
2.2	Instructions	50/60 mins	T2, R1
2.3	Addressing modes	50/60 mins	T2, R1
2.4	Assembler directives	50/60 mins	T2, R1
2.5	Writing simple programs with an assembler	50/60 mins	T2, R1
2.6	Writing simple programs with an assembler	50/60 mins	T2, R1
2.7	Assembly language program development tools	50/60 mins	T2, R1
2.8	Assembly language program development tools	50/60 mins	T2, R1
UNIT-3			
3.0	8086 Interfacing: Semiconductor memories interfacing (RAM, ROM)	50/60 mins	T1
3.1	Intel 8255 programmable peripheral interface	50/60 mins	T1
3.2	Interfacing switches and LEDS	50/60 mins	T1
3.3	Interfacing seven segment displays	50/60 mins	T1
3.4	software and hardware interrupt applications	50/60 mins	T1
3.5	software and hardware interrupt applications	50/60 mins	T1
3.6	Intel 8251 USART architecture	50/60 mins	T1
3.7	Intel 8251 USART interfacing	50/60 mins	T1
3.8	Intel 8237a DMA controller	50/60 mins	T1
3.9	Stepper motor	50/60 mins	T1
3.10	A/D and D/A converters	50/60 mins	T1
3.11	Need for 8259 programmable interrupt controllers	50/60 mins	T1
UNIT-4			
4.0	Intel 8051 MICROCONTROLLER Architecture	50/60 mins	T1, T2, R1
4.1	Hardware concepts	50/60 mins	T1, T2, R1
4.2	Input/output ports and circuits	50/60 mins	T1, T2, R1
4.3	Input/output ports and circuits	50/60 mins	T1, T2, R1
4.4	External memory	50/60 mins	T1, T2, R1

4.5	Counters/timers,	50/60 mins	T1, T2, R1
4.6	Serial data input/output	50/60 mins	T1, T2, R1
4.7	Interrupts	50/60 mins	T1, T2, R1
4.8	Assembly language programming: Instructions	50/60 mins	T1, T2, R1
4.9	Addressing modes	50/60 mins	T1, T2, R1
4.10	Simple programs	50/60 mins	T1, T2, R1
4.11	Simple programs	50/60 mins	T1, T2, R1
4.12	Interfacing to 8051: A/D and D/A converters	50/60 mins	T1, T2, R1
4.13	Stepper motor interface	50/60 mins	T1, T2, R1
4.14	Keyboard, LCD interfacing	50/60 mins	T1, T2, R1
4.15	Traffic light control	50/60 mins	T1, T2, R1
UNIT-5			
5.0	ARM Architectures and Processors: ARM Architecture	50/60 mins	T2, R2
5.1	ARM Processors Families	50/60 mins	T2, R2
5.2	ARM Processors Families	50/60 mins	T2, R2
5.3	ARM Cortex-M Series Family	50/60 mins	T2, R2
5.4	ARM Cortex-M Series Family	50/60 mins	T2, R2
5.5	ARM Cortex-M3 Processor Functional Description	50/60 mins	T2, R2
5.6	ARM Cortex-M3 Processor Functional Description	50/60 mins	T2, R2
5.7	Functions	50/60 mins	T2, R2
5.8	Interfaces	50/60 mins	T2, R2

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Evaluation Scheme:

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Mid-Sem Grading:

Mid-sem marks shall be displayed after two evaluation components. (Refer Academic calendar for schedule).

Note: A student will likely be detained , if he / she doesn't appear / appear for the sake of appearing for the evaluation components / scoring zero in internal marks.

EC No	Evaluation Components	Duration Min	Marks	Weightage	Date & Time	Venue
1	MID – I	90	10	80% from best Mid 20% from other Mid		TO BE ANNOUNCED
	MID – II		10			
2	QUIZ – I	20	10			
	QUIZ – II		10			
3	ASSIGNMENT – I	.....	5			
	ASSIGNMENT – II	.....	5			
4	SEM EXAMS	3 hrs.		75%		

Attendance policies:

Attendance: Every student is expected to be responsible for regularity of the his/her attendance in class rooms and laboratories, to appear in scheduled tests and examinations and fulfill all other tasks assigned to him/her. Student should have a minimum of 75% of attendance in course to be eligible to appear for the University Examinations. As per the Govt. norms for reimbursement it is mandatory to have 75% biometric aadhar linked attendance to be eligible to scholarship.

Chamber consultation hours: - during **free period** the student can contact in my chamber for consultation regarding course.

General Instructions:

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Notices:

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Contact details

Prof. T. Hemalatha , Assistant Professor , Chamber No:215 email: tankala.hema455@gmail.com

T. Hema Latha

Instructor-in-Charge

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Lingayas Institute of Management and Technology

(Approved by A I C T E - New Delhi & Affiliated to J N T University Kakinada)
Madalavarigudem, Vijayawada.

INSTRUCTION DIVISION
III-YEAR II-SEMESTER 2020– 2021
(BIOMETRIC SYSTEM OF ATTENDENCE IS MANDATORY AS PER NORMS OF GOVT. OF AP AND JNTUK)

Course Handout

In addition to Part 1 (General Handout for all courses appended to the Time Table) this portion further specific details regarding the course.

L	T	P	C
4	1	0	3

Course Code : **R1632043**

Course Title : **VLSI DESIGN**

Instructor-in-charge : **Prof. J. Sambasivarao Rao**

Course Objectives:

The student will be made

1. Basic characteristics of MOS transistor and examines various possibilities for configuring inverter circuits and aspects of latch-up are considered.
2. Design processes are aided by simple concepts such as stick and symbolic diagrams but the key element is a set of design rules, which are explained clearly.
3. Basic circuit concepts are introduced for MOS processes we can set out approximate circuit parameters which greatly ease the design process.

Outcomes:

At the end of this course the student can able to:

1. Understand the properties of MOS active devices and simple circuits configured when using them and the reason for such encumbrances as ratio rules by which circuits can be interconnected in silicon.
2. Know three sets of design rules with which n-MOS and CMOS designs may be fabricated.
3. Understand the scaling factors determining the characteristics and performance of MOS circuits in silicon.

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SYLLABUS

UNIT-I: Introduction and Basic Electrical Properties of MOS Circuits: Introduction to IC technology, Fabrication process: n-MOS, p-MOS and CMOS, Ids versus Vds Relationships, Aspects of MOS transistor Threshold Voltage, MOS transistor Trans, Output Conductance and Figure of Merit, n-MOS Inverter, Pull-up to Pull-down Ratio for n-MOS inverter driven by another n-MOS inverter, and through one or more pass transistors, Alternative forms of pull-up, The CMOS Inverter, Latch-up in CMOS circuits, Bi-CMOS Inverter, Comparison between CMOS and Bi-CMOS technology.

UNIT-II: MOS and Bi-CMOS Circuit Design Processes: MOS Layers, Stick Diagrams, Design Rules and Layout, General observations on the Design rules, 2μm Double Metal, Double Poly, CMOS/Bi-CMOS rules, 1.2μm Double Metal, Double Poly CMOS rules, Layout Diagrams of NAND and NOR gates and CMOS inverter, Symbolic Diagrams Translation to Mask Form.

UNIT-III: Basic Circuit Concepts: Sheet Resistance, Sheet Resistance concept applied to MOS transistors and Inverters, Area Capacitance of Layers, Standard unit of capacitance, some area Capacitance Calculations, The Delay Unit, Inverter Delays, driving large capacitive loads, Propagation Delays, Wiring Capacitances, Choice of layers, Scaling of MOS Circuits: Scaling models and scaling factors, Scaling factors for device parameters, Limitations of scaling, Limits due to sub threshold currents, Limits on logic levels and supply voltage due to noise and current density, Switch logic, Gate logic.

UNIT-IV: Chip Input and Output circuits: ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip clock Generation and Distribution. Design for Testability: Fault types and Models, Controllability and Observability, Ad Hoc Testable Design Techniques, Scan Based Techniques and Built-In Self- Test techniques.

UNIT-V: FPGA Design: FPGA design flow, Basic FPGA architecture, FPGA Technologies, FPGA families- Altera Flex 8000FPGA, Altera Flex 10FPGA, Xilinx XC4000 series FPGA, Xilinx Spartan XL FPGA, Xilinx Spartan II FPGAs, Xilinx Vertex FPGA. Case studies: FPGA Implementation of Half adder and full adder.

Introduction to synthesis: Logic synthesis, RTL synthesis, High level Synthesis.

UNIT-VI: Introduction to Low Power VLSI Design: Introduction to Deep submicron digital IC design, Low Power CMOS Logic Circuits: Over view of power consumption, Low –power design through voltage scaling, Estimation and optimization of switching activity, Reduction of switching capacitance, Interconnect Design, Power Grid and Clock Design.

Study Material:

Text Books:

1. Essentials of VLSI Circuits and Systems - Kamran Eshraghian, Douglas and A. Pucknell and Sholeh Eshraghian, Prentice-Hall of India Private Limited, 2005 Edition.

2. CMOS Digital Integrated Circuits Analysis and Design- Sung-Mo Kang, Yusuf Leblebici, Tata McGrawHill Education, 2003.

References: 1. Advanced Digital Design with the Verilog HDL, Michael D.Ciletti, Xilinx Design Series, Pearson Education 2. Analysis and Design of Digital Integrated Circuits in Deep submicron Technology, 3'rd edition, David Hodges.

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UNIT-TOPIC	TOPIC	TEACHING AID	REFERENCE
1.0	Introduction to IC technology **Fabrication process:** n-MOS, p-MOS and CMOS	PPT	T1
1.2	I_{ds} versus V_{ds} Relationships, Aspects of MOS transistor Threshold Voltage	BLACK BOARD	T1
1.4	MOS transistor Trans, Output Conductance and Figure of Merit.	PPT	T1
1.6	n-MOS Inverter, Pull-up to Pull-down Ratio for n-MOS inverter, Driven by another n-MOS inverter, and through one or more pass transistors.	BLACK BOARD	T1
1.8	Alternative forms of pull-up, The CMOS Inverter, Latch-up in CMOS circuits, Bi-Cmos inverter, comparison between cmos and b-cmos technology	PPT	T1
2.0	MOS Layers, Stick Diagrams, Design Rules and Layout	PPT	T1
2.2	General observations on the Design rules,2μm Double Metal, Double Poly	PPT	T1
2.4	CMOS/Bi-CMOS rules,1.2μm Double Metal, Double Poly CMOS rules	PPT	T1
2.6	Layout Diagrams of NAND and NOR gates	PPT	T1
2.8	CMOS inverter Symbolic Diagrams-Translation to Mask Form	PPT	T1
3.0	Sheet Resistance, Sheet Resistance concept applied to MOS transistors and Inverters	PPT	T1
3.2	Area Capacitance of Layers, Standard unit of capacitance, The Delay Unit, Inverter Delays	PPT	T1
3.4	Driving large capacitive loads, Some area Capacitance Calculations, Propagation Delays, Wiring Capacitances, Choice of layers	PPT	T1
3.6	Scaling models and scaling factors, Scaling factors for device parameters, Limitations of scaling	PPT	T1
3.8	Limits due to sub threshold currents, Limits on logic levels	PPT	T1
4.0	ESD Protection, Input Circuits, Output Circuits	PPT	T2

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4.2	L(di/dt) Noise, On-Chip clock Generation and Distribution	PPT	T2
4.4	Fault types and Models	PPT	T2
4.6	Controllability and Observability, Ad Hoc Testable Design Techniques	PPT	T2
4.8	Scan Based Techniques, Built-In Self -Test techniques	PPT	T2
5.0	FPGA design flow, Basic FPGA architecture	PPT	T1
5.2	FPGA TECHNOLOGIES, FPGA families-Altera Flex 8000FPGA	PPT	T1
5.4	Altera Flex 10FPGA, Xilinx XC4000 series FPGA, Xilinx Spartan XL FPGA	PPT	T1
5.6	Xilinx Spartan II FPGAs, Xilinx Vertex FPGA, Case studies: FPGA Implementation of Half adder and full adder	PPT	T1
5.8	Logic synthesis, RTL synthesis, High level Synthesis	PPT	T1
6.0	Introduction to Deep submicron digital IC design, Over view of power consumption	PPT	T2
6.2	Low –power design through voltage scaling Estimation and optimization of switching activity	PPT	T2
6.4	Reduction of switching capacitance	PPT	T2
6.6	Interconnect Design	PPT	T2
6.8	Power Grid and Clock Design	PPT	T2

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LESSON PLAN

WEEK NO	FROM	TO	TOPIC NAME	NO OF HRS
			ORINETATION	2
1	1.0	1.2	**UNIT-I: Introduction and Basic Electrical Properties of MOS Circuits:** Introduction to IC technology, Fabrication process: nMOS, p-MOS and CMOS. Ids versus Vds Relationships, Aspects of MOS transistor Threshold Voltage	3
2	1.4	1.8	MOS transistor Trans, Output Conductance and Figure of Merit. n-MOS Inverter, Pull-up to Pull-down Ratio for n-MOS inverter, Driven by another n-MOS inverter, and through one or more pass transistors. Alternative forms of pull-up. The CMOS Inverter, Latch-up in CMOS circuits. Bi-Cmos inverter, comparison between cmos and b-cmos technology	5
3	2.0	2.2	**UNIT-II: MOS and Bi-CMOS Circuit Design Processes:** MOS Layers, Stick Diagrams, Design Rules and Layout General observations on the Design rules.2µm Double Metal, Double Poly	5
4	2.4	2.6	CMOS/Bi-CMOS rules,1.2µm Double Metal, Double Poly CMOS rules, Layout Diagrams of NAND and NOR gates, CMOS inverter Symbolic Diagrams- Translation to Mask Form	5
5	2.8	2.8	Limits due to sub threshold currents, Limits on logic levels	3
6	3.0	3.2	**UNIT-III:** Sheet Resistance, Sheet Resistance concept applied to MOS transistors and Inverters, AreaCapacitance of Layers, Standard unit of capacitance, The Delay Unit, Inverter Delays	5
7	3.4	3.6	Driving large capacitive loads, Some area Capacitance Calculations, Propagation Delays, Wiring Capacitances, Choice of layers, Scaling models and scaling factors, Scaling factors for device parameters, Limitations ofscaling	4
8	3.8	3.8	Limits due to sub threshold currents, Limits on logic levels	
9			MID-I EXAMS	
10	4.0	4.2	**UNIT-IV:** ESD Protection, Input Circuits, Output Circuits L(di/dt) Noise, On-Chip clock Generation and Distribution	4
11	4.4	4.6	Fault types and Models, Controllability and Observability, Ad Hoc Testable Design Techniques	

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12	4.8	4.8	Scan Based Techniques, Built-In Self -Test techniques	3
13	5.0	5.2	UNIT-V: FPGA design flow, Basic FPGA architecture FPGA TECHNOLOGIES, FPGA families- Altera Flex 8000FPGA	3
14	5.4	5.8	Altera Flex 10FPGA, Xilinx XC4000 series FPGA, Xilinx Spartan XL FPGA Xilinx Spartan IIFPGAs, Xilinx Vertex FPGA, Case studies: FPGA Implementation of Half adder and full adder Logic synthesis, RTL synthesis, High level Synthesis	3
15	6.0	6.2	UNIT-VI: Introduction to Deep submicron digital IC design. Over view of power consumption. Low –power design through voltage scaling Estimation and optimization of switching activity	3
16	6.4	6.8	Reduction of switching capacitance, Interconnect Design,Power Grid and Clock Design	3

EVALUATION SCHEME:

EC No	Evaluation Components	Duration Min	Marks	Weightage	Date & Time	Venue
1	MID – I		15	80% from best Mid 20% from other Mid	13-05-2021 to 23-05-2021	TO BE ANNOUNCED
	MID – II	3Hrs	15		23-07-2021 to 28-07-2020	
2	QUIZ – I		10		13-05-2021 to 23-05-2020	
	QUIZ – II		10		23-07-2021 to 28-07-2020	
3	ASSIGNMENT – I		5			
	ASSIGNMENT – II		5			
4	SEM EXAMS	3 hrs.	70%		04-08-2021 to 18-08-2021	

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Prof. J SAMBASIVARAO, Assistant Professor, Chamber No:214, email: sambasiva9841@gmail.com

Instructor-in-Charge

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